Specification Amendments

Amend the paragraph beginning on line 14 of page 9 and ending on line 4 of page 10 as follows:

In an alternate embodiment illustrated in Fig. 2, memory system 2 includes two (or more) DRAM banks which are interleaved, allowing pipelined or partitioned operation, wherein one bank may be refreshed while the other is accessed for normal operation. As in the embodiment shown in Fig. 1, the memory controller 12 generates a separate chip select signal for each WEDAC unit. The WEDAC0 16 receives a predetermined number, *a*, of data bits, while the WEDAC1 18 receives a predetermined number, *b*, of data bits, where $x = a + b$ and *a* and *b* are not necessarily equal. Each WEDAC unit calculates an appropriate number of check bits according to the number of data bits received. The WEDAC0 16 generates *s* check bits to form a code word having $(a + s)$ bits for storage in the DRAM0 24. Similarly, WEDAC1 18 generates *t* check bits to form a code word having $(b + t)$ bits, which is then stored in DRAM1 26. Note that chip select signals, CS0 and CS1 are each coupled to DRAM0 24 and DRAM1 26, respectively. In this way, the memory system 2 may "scrub" the DRAM0 24 while the DRAM1 26 is in normal operating mode and *vise versa*. As one DRAM may be scrubbed in isolation, the scrubbing operation does not impact the speed or function of the other DRAM. Note that DRAM0 24 and DRAM1 26 may be banks or tiles within a single chip memory, or may be discrete memory devices. Such a tiled memory system and a method for scrubbing are disclosed in our copending patent application entitled "METHOD AND APPARATUS FOR REFRESHING AND SCRUBBING A DYNAMIC MEMORY " by Longwell et al., ~~having Attorney Docket No. JMS008-00~~Application Serial No. 09/313,876, filed May 18, 1999, but now abandoned, and assigned to the assignee hereof, which is expressly incorporated herein by reference.